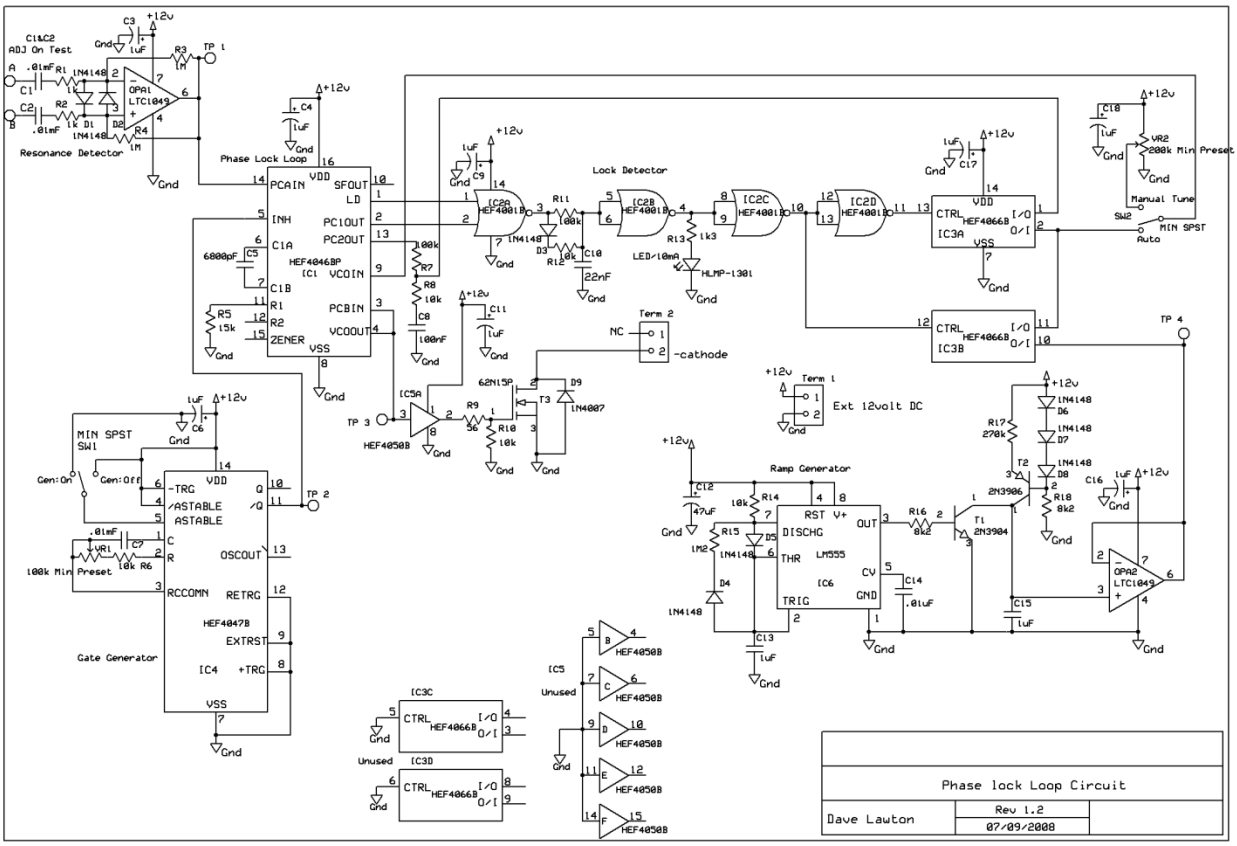
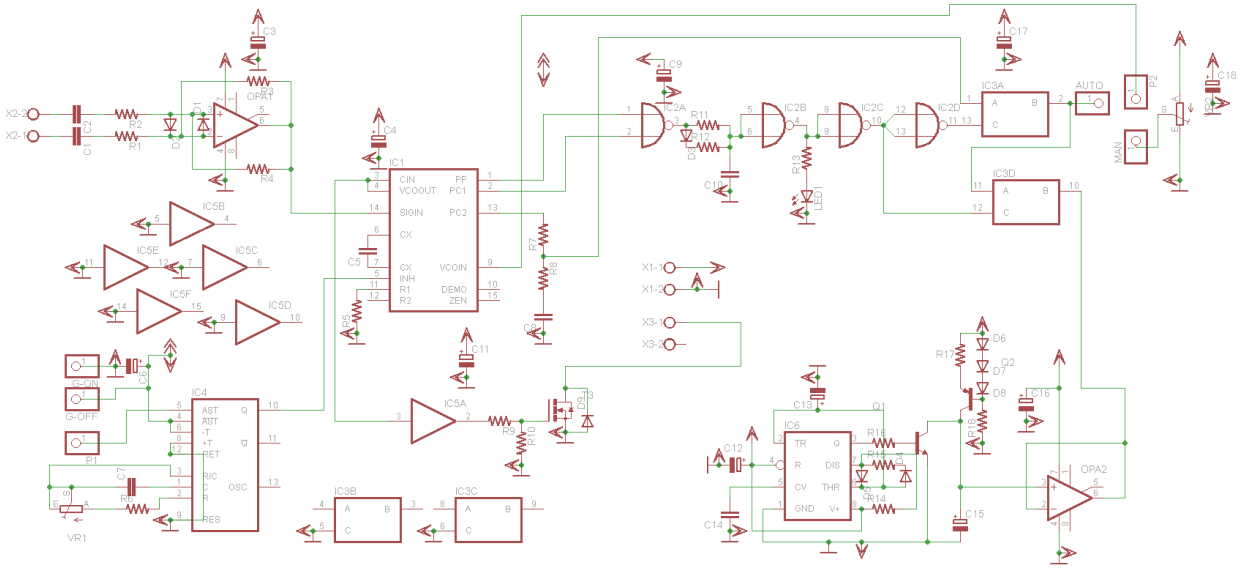
DAVE LAWTON PHASE LOCK LOOP DEVICE

Part Value	Description	
C1, C2, C7 & C14	0.01uF (10nF, 10,000pF or 103)	4off
C3, C4, C6, C9, C11, C13 C15, C16, C17 & C18	1uF	10off
C5	0.0068uF (6.8nF or 6800pF)	1off
C8	0.1uF (100nF or 100,000pF)	1off
C10	0.022uF (22nF or 22000pF)	1off
C12	47uF	1off
D1-8	1N4148	8off
D9	1N4007	1off
IC1	CD4046BE	1off
IC2	HCF4001BE	1off
IC3	HCF4066BE	1off
IC4	HCF4047BE	1off
IC5	HCF4050BE	1off
IC6	LM555N	1off
LED1	Red 5mm	1off
OPA1 & 2	LTC1049	2off
Q1	2N3904	1off
Q2	2N3906	1off
R1 & R2	1k	2off
R3 & R4	1M	2off
R5	15k	1off
R6, R8, R10, R12 & R14	10k	5off
R7 & R11	100k	2off
R9	56R	1off
R13	1k2	1off
R15	1M2	1off
R16 & R18	8k2	2off
R17	270k	1off
T3	IRFP240	1off
VR1	100k trimmer	1off
VR2	200k trimmer	1off
8pin DIL socket		3off
14pin DIL socket		3off
16pin DIL socket		2off
Sub-miniature SPDT switch		2off
2 way terminal blocks		3off
PCB		1off

The circuit diagram below is Dave's original sent to me in Express PCB format, it does contain one error in that the link between the PLL chip and the gate generator should go to pin 10 of the gate generator as in my circuit below.





For a view on how it should be installed in conjunction with your cell please refer to Patrick Kelly's document to be found at www.free-energy-info.co.uk/D14.pdf on p.27of the current version (21/05/10).

The finished PCB should look something like this.